



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Applicant : Alex Kalnitsky, et al Docket No : 93-C-32
Serial No : 08/163,043 Group : 1109
Filed : December 6, 1993 Examiner : T. Dang
For : Enhanced Planarization Technique for an Integrated Circuit

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GROUP 1100

SUPPLEMENTAL DECLARATION

Hon. Commissioner of Patents
and Trademarks
Washington, D.C.

Dear Sir:

I, Alex Kalnitsky, and Yih-Shung Lin, as below-named inventors in the application for letters patent for an improvement in Enhanced Planarization Technique for an Integrated Circuit, Serial No. 08/163,043, filed in the United States Patent and Trademark Office on or about the 6th day of December, 1993, declare that my residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought;

I have reviewed and understand the contents of the above-identified specification, including the subject matter of the following amendment(s) mailed on November 1, 1994;

that said subject matter, including the claims as amended, was part of my invention before the filing of the original application, above identified, for such invention; and that I acknowledge my duty to disclose information of which I am aware which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Signature: A. Kalnitsky

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Date of Signature: July 4, 1995

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